Notice of Allowability	Application No.	Applicant(s)
	10/645,660	FAYNEH ET AL.
	Examiner	Art Unit
	Dipakkumar Gandhi	2138

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 3/20/2006.
2. ☒ The allowed claim(s) is/are 1, 2, 6, 8-12, 14-16, 19-22, 24-40, which are renumbered as 1-32.
3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Allowable Subject Matter

1. Claims 1, 2, 6, 8-12, 14-16, 19-22, 24-40 are allowed over the prior arts of record. Claims 3-5, 7, 13, 17-18, 23 are cancelled.

2. Applicants' amendment (including amended claims) filed on 3/20/2006 has been entered.

3. The following is an examiner's statement of reasons for allowance:

The present invention pertains to a system and method for performing duty-cycle correction of clock and other frequency signals.

The claimed invention (claim 1 as representative) recites features such as:"...a measurement circuit to measure duty-cycle distortion in a first clock signal, the measurement circuit including: (a) a single-input charge pump driven by the first clock signal, (b) a loop filter to output a voltage corresponding to an average of current from the charge pump over a predetermined time, and (c) a bias generator to generate an analog correction signal based on the voltage output from the loop filter; and a correction circuit to dynamically adjust a delay of at least one edge of a second clock signal based on the analog correction signal received from the bias generator to reduce the duty-cycle distortion in the first clock signal, the first clock signal being generated based on the second clock signal."

The prior art of record (Kizer et al. US 6,967,514 B2) teach a method for adjusting, correcting or maintaining a clock's duty cycle. An incremental error signal is generated in response to the clock signal, and a cumulative error signal is generated in response to the incremental error signal. The duty cycle of the clock signal is adjusted in response to the cumulative error signal (col. 3, lines 8-13, Kizer et al.).

Davis et al. (US 6,981,185 B1) teach an apparatus for correcting duty cycle error in a data transmission system is provided. The apparatus includes an oversampler being configured to oversample an input signal, and an accumulator coupled to the oversampler. The accumulator generates an accumulated high bit signal and an accumulated low bit signal from the oversampled input signal received from the oversampler. The apparatus also includes a comparator coupled to the accumulator. The comparator receives an accumulated high bit signal and an accumulated low bit signal from the accumulator. The comparator compares an amount of the accumulated high bit signal and the accumulated low bit signal.

The apparatus further includes a successive approximation register (SAR) logic coupled to the comparator where the SAR logic receives a compared signal from the comparator and determines a duty cycle error (col. 4, lines 38-53, Davis et al.).

Lu (US 6,100,735) teaches delay-locked loop (DLL). Lu teaches that when the phase of DCLK (final delayed clock) varies from that of ICLK (input clock), phase comparator 14 commands charge pump 16 to adjust the bias voltage to buffers 12. The delay through buffers 12 changes until the delay through the series of buffers 12 is exactly one period of ICLK (col. 1, lines 61-65, Lu). Lu teaches that an input clock is generated from a constant-frequency source such as from a crystal oscillator (col. 1, lines 37-38, Lu). In claim 1, the first clock signal is generated based on the second clock signal.

Maneatis (US 5,727,037) teaches a system and method for using self-biased circuits to reduce phase jitter and phase offset in phase locked loops (abstract, Maneatis). Maneatis teaches that charge pumps 104, 106 each have three inputs and one output (fig. 1, col. 4, lines 40-41, Maneatis). In claim 1, charge pump has a single-input.

Ishikawa et al. (US 5,991,221) teach a microcomputer incorporating a flash memory, which is erased and programmed electrically in a stable manner (abstract, Ishikawa et al.).

Van der Veer et al. (US 6,924,480 B2) teach a technique employing volume conductive electrodes for the generation of linear or non-linear electric fields for devices used in charged ion optics (abstract, Van der Veer et al.).

Schultz et al. (US 6,191,613 B1) teach that a programmable logic device (PLD), such as a field programmable gate array (FPGA), includes an integrated delay-locked loop that produces a lock signal internal to the FPGA (abstract, Schultz et al.).

However the prior arts of record do not teach a measurement circuit to measure duty-cycle distortion in a first clock signal, the measurement circuit including: (a) a single-input charge pump driven by the first clock signal, (b) a loop filter to output a voltage corresponding to an average of current from the charge pump over a predetermined time, and (c) a bias generator to generate an analog correction signal based on the voltage output from the loop filter; and a correction circuit to dynamically adjust a delay of at least one edge of a second clock signal based on the analog correction signal received from the bias generator

to reduce the duty-cycle distortion in the first clock signal, the first clock signal being generated based on the second clock signal.

Hence, the prior arts of record do not anticipate nor render obvious the claimed inventions. Thus, claim 1 is allowable over the prior arts of record. Claims 2, 6, 8, 9, 26, 27, 30-40 are allowed because of the combination of additional limitations and the limitations listed above.

- Independent claims 10, 19, 24 recite similar features as in claim 1. Thus, independent claims 10, 19, 24 are allowable over the prior arts of record. Claims 11, 12, 14-16, 20-22, 25, 28, 29 are allowed because of the combination of additional limitations and the limitations listed above.
- Thus, claims 1, 2, 6, 8-12, 14-16, 19-22, 24-40 are allowed over the prior arts of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

D. Gandhi

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